

Patent and Trademark Office

COMMISSIONER OF PATENTS AND TRADEMARKS Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAME	DINVENTOR		ATTORNEY DOCKET NO.
09/539,458	03/30/00	CHANG		М	1346P/DA0102
		haharinin zonen e		EXAMINER	
JOSEPH A SAWYER JR		MMC2/0925		PHAM, H	1
SAWYER LAW GROUP LLP			•	ART UNIT	PAPER NUMBER
P 0 BOX 514	18				
PALO ALTO C	A 94303			2814	
				DATE MAILED:	
					09/25/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

		Application No.	Applicant(s)				
Office Action Summary		09/539,458	CHANG ET AL.				
		Examiner	Art Unit				
		Hoai V Pham	2814				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status							
1) 🖂	Responsive to communication(s) filed on 09 J	ulv 2001 .					
2a)□		s action is non-final.					
3)□							
Dispositi	on of Claims						
4)⊠ Claim(s) <u>1-16</u> is/are pending in the application.							
4a) Of the above claim(s) $8-16$ is/are withdrawn from consideration.							
5) Claim(s) is/are allowed.							
6)⊠ Claim(s) <u>1-7</u> is/are rejected.							
7)	Claim(s) is/are objected to.		•				
8) Claim(s) are subject to restriction and/or election requirement.							
Application	on Papers						
9)☐ The specification is objected to by the Examiner.							
10) The drawing(s) filed on is/are: a) □ accepted or b) □ objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
11) ☐ The proposed drawing correction filed on is: a) ☐ approved b) ☐ disapproved by the Examiner.							
If approved, corrected drawings are required in reply to this Office action.							
12) The oath or declaration is objected to by the Examiner.							
Priority under 35 U.S.C. §§ 119 and 120							
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).							
a) All b) Some * c) None of:							
1. Certified copies of the priority documents have been received.							
2. Certified copies of the priority documents have been received in Application No							
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 							
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).							
 a) ☐ The translation of the foreign language provisional application has been received. 15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121. 							
Attachment(s)							
2) Notice	of References Cited (PTO-892) of Draftsperson's Patent Drawing Review (PTO-948) ation Disclosure Statement(s) (PTO-1449) Paper No(s)	5) Notice of Informal P	(PTO-413) Paper No(s) atent Application (PTO-152)				

Art Unit: 2814

DETAILED ACTION

Election/Restrictions

Applicant's election of claims 1-7 in Paper No. 3 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (hereinafter AAPA) in view of Paterson et al. [U.S. Pat. 5,065,220].

Art Unit: 2814

Applicant Admitted Prior Art discloses a flash memory device comprising:

a plurality of gate stacks including a plurality of floating gates (62) and a plurality
of control gates (66) disposed on a semiconductor substrate;

at least one component including a polysilicon layer (76) having a top surface; an insulating layer (80) covering the plurality of gate stacks, the at least one component, the insulating layer having a plurality of contact holes (82, 84, 86) and a conductor filling the plurality of contact holes.

Applicant Admitted Prior Art does not teach a silicide on the top surface of the polysilicon layer of the at least one component, and the insulating layer etching step using the silicide as an etch stop layer to ensure that the insulating etching step does not etch through the polysilicon layer. However, Paterson et al. shows that it is conventional in the art to have a device with a silicide (14) on top surface of the polysilicon layer (12) wherein the contact hole (26) being formed through the insulating layer (16) and stopped at the silicide film (14) to improve stability of the underlying polysilicon (see figures 1-2, cols. 2-5). Therefore, it would have been obvious to the skilled in the art to use silicide on the top surface of the polysilicon layer in the Applicant Admitted Prior Art device to provide a better device with an improved stabibity of the polysilicon and a further reduced resistance of the polysilicon.

With respect to claim 2, Paterson et al. shows that the silicide further includes a titanium silicide (see col. 3, lines 45-46).

With respect to claim 3, Paterson et al. does not particularly mention that the silicide further includes a cobalt silicide. However, Paterson et al. shows that any

Art Unit: 2814

refractory metal can be used for silicide (see col. 3, lines 45+). Since cobalt is well known refractory metal, it would have been obvious to use colbalt silicide in the device of Applicant Admitted Prior Art in view of Paterson et al.

With respect to claim 6, Applicant Admitted Prior Art discloses that the plurality of gate stacks further include a plurality of spacers (74) (see figure 2).

With respect to claim 7, Applicant Admitted Prior Art discloses that at least one field oxide region (54), the at least one component being located on the at least one field oxide region (see figure 2).

With respect to claims 4, 5 and 6, Paterson et al. shows that oxide-nitride-oxide layers (20, 22) on the polysilicon (12) (see col. 4, lines 30-38).

Note that process limitation in claims 1, 5 and 6 (oxide-nitride-oxide layer is removed prior to formation of the silicide; removed during a second polysilicon layer etching step or removed after formation of the plurality of spacers.) do not carry weight in a claim drawn to structure. *In re Thorpe*, 227 USPQ 964 (Fed. Cir. 1985). In addition, a "product by process" limitation is directed to the product per se, no matter how actually made, in re Hirao, 190 USPQ 15 and 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90; and *In re Marosi et al.*, 218 USPQ 289; all of which made clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product by a new method is not patentable as a product, whether claimed in "product by process" claims or not.

Art Unit: 2814

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai V Pham whose telephone number is 703-308-6173. The examiner can normally be reached on 6:30A.M. - 6:00P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

HP Hoai Pham September 13, 2001

OLIK CHAUDHURI SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2800

Page 5